REMARKS

Claims 1-10 and 12-20 are pending herein. Claims 7-10, 15 and 16 are withdrawn.

By this Amendment, claim 1 is amended to further clarify comparison of the two pairs of signals. Thus, no new matter is added by this Amendment.

Applicant appreciates the courtesies shown to Applicant's representative by Examiner Hu in the October 21, 2004 personal interview. Applicant's separate record of the substance of the interview is incorporated into the following remarks.

During the October 21 interview, the Examiner agreed that the present comparator which compares the phase of the signal across one of the two layers with the phase of the signal across the other of the two layers is a feature not taught or suggested by Matsumoto. However, the Examiner requested that this feature be better clarified in the claims. Thus, as suggested by the Examiner, claim 1 is amended to further recite "wherein the comparator compares a phase of a signal across the input and common electrodes with the phase of the signal across the output and common electrodes to provide said logic state indication."

Furthermore, during the October 21 interview, the Examiner asserted that the feature in the claims of the layers clamped together to enhance the amplitude of a voltage generated across one of the two layers is disclosed by Matsumoto. Specifically, the Examiner stated that a passivation layer, as taught by Matsumoto, naturally forms a clamping environment. Thus, the Examiner alleged that such a feature is inherent in Matsumoto. However, the Examiner also indicated that further clarifying this feature may be sufficient to overcome the 35 U.S.C. §102(b) rejection of claim 1 in view of Matsumoto.

In this regard, Matsumoto fails to disclose or anywhere mention a passivation layer. Furthermore, a passivation layer would have a clamping effect only by shrinking. Shrinking of this layer would depend on the material used. There is no indication that the layer taught by

Matsumoto may shrink. Thus, as to the specific disclosure of the passivation material, clamping can not be assumed to take place or to be taught by Matsumoto.

Furthermore, even if the passivation layer of Matsumoto did shrink, its clamping effect would depend on the height/width ratio of the device. A low height/width ratio of the device would have a very low clamping effect. Thus, in the absence of such a ratio, any clamping effect would be unquantifiable. Further still, to have a clamping effect, the passivation layer would have to be on top of the entire device. Such a layer would normally be applied to the wafer used, hence it would not be likely that the layer of Matsumoto would act as a clamp.

For the reasons discussed above, it is not inherent that Matsumoto teaches or suggests a clamping of its memory devices with the use of the passivation layer.

Accordingly, as acknowledged by the Examiner, the rejection of claim 1 under 35 U.S.C. §102(b) as allegedly being anticipate by U.S. Patent No. 3,754,214 (Matsumoto) is overcome.

Reconsideration and withdrawal of the rejection is thus respectfully requested.

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-10 and 12-20 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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